(12) UK Patent Application (19) GB (11) 2 137 811 A

(43) Application published 10 Oct 1984

(21) Application No 8406974

(22) Date of filing 16 Mar 1984

(30) Priority data

(31) 477012 (32) 21 Mar 1983 (33) US

(51) INT CL³
H01L 27/10 29/52 29/78

(52) Domestic classification
H1K 11A3 11B3 11C1A 11C4 11D1 11D 1BC 1CA 4C11 4C1U 4C2B 4C2U 4F1C 4F20 HAX

(56) Documents cited
None

(58) Field of search
H1K

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(54) High power MOSFET with direct connection from connection pads to underlying silicon

(57) The gate electrode pad (12, Fig. 1) and the source electrode pad 11 of a high power MOSFET or diode type device are supported atop an oxide layer 42, and the peripheral regions of the source electrode which surround the areas of the gate and source pads are connected at a plurality of points e.g. 82 around their peripheries through the oxide layer to the underlying silicon 16. This enables rapid collection of minority carriers which were weakly injected into the region surrounding the pads when a junction beneath the pads was forward-biased.

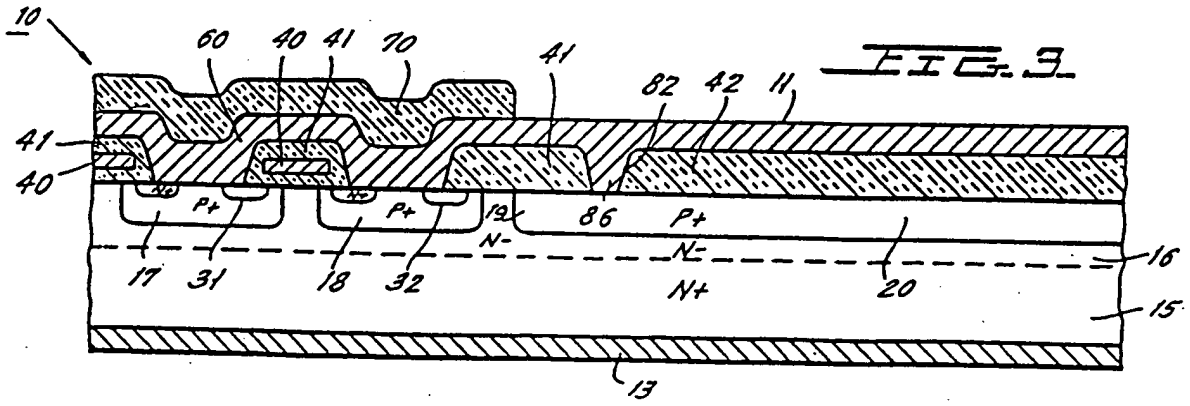

FIG. 3.

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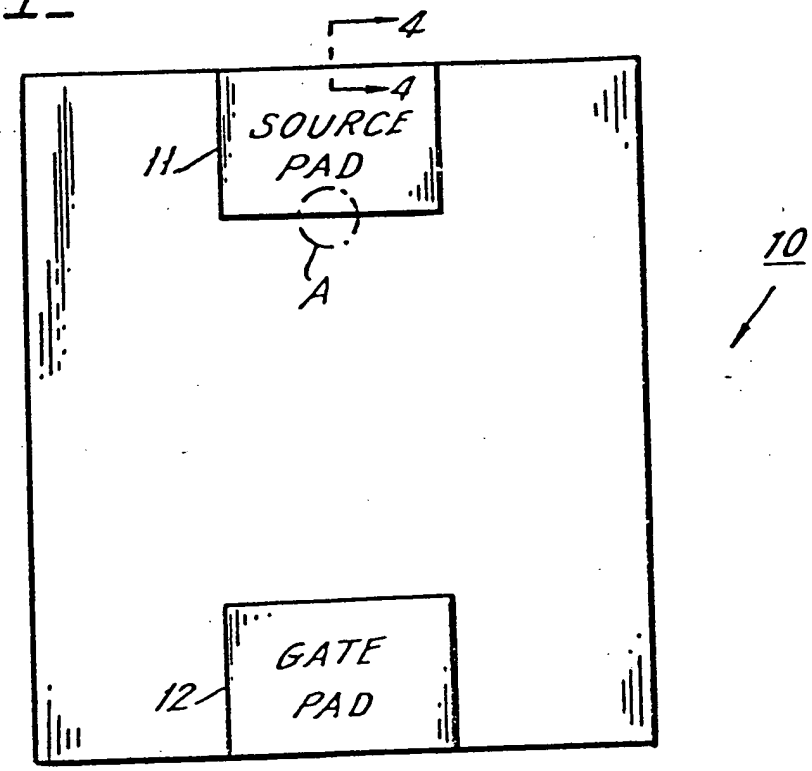
FIG. 1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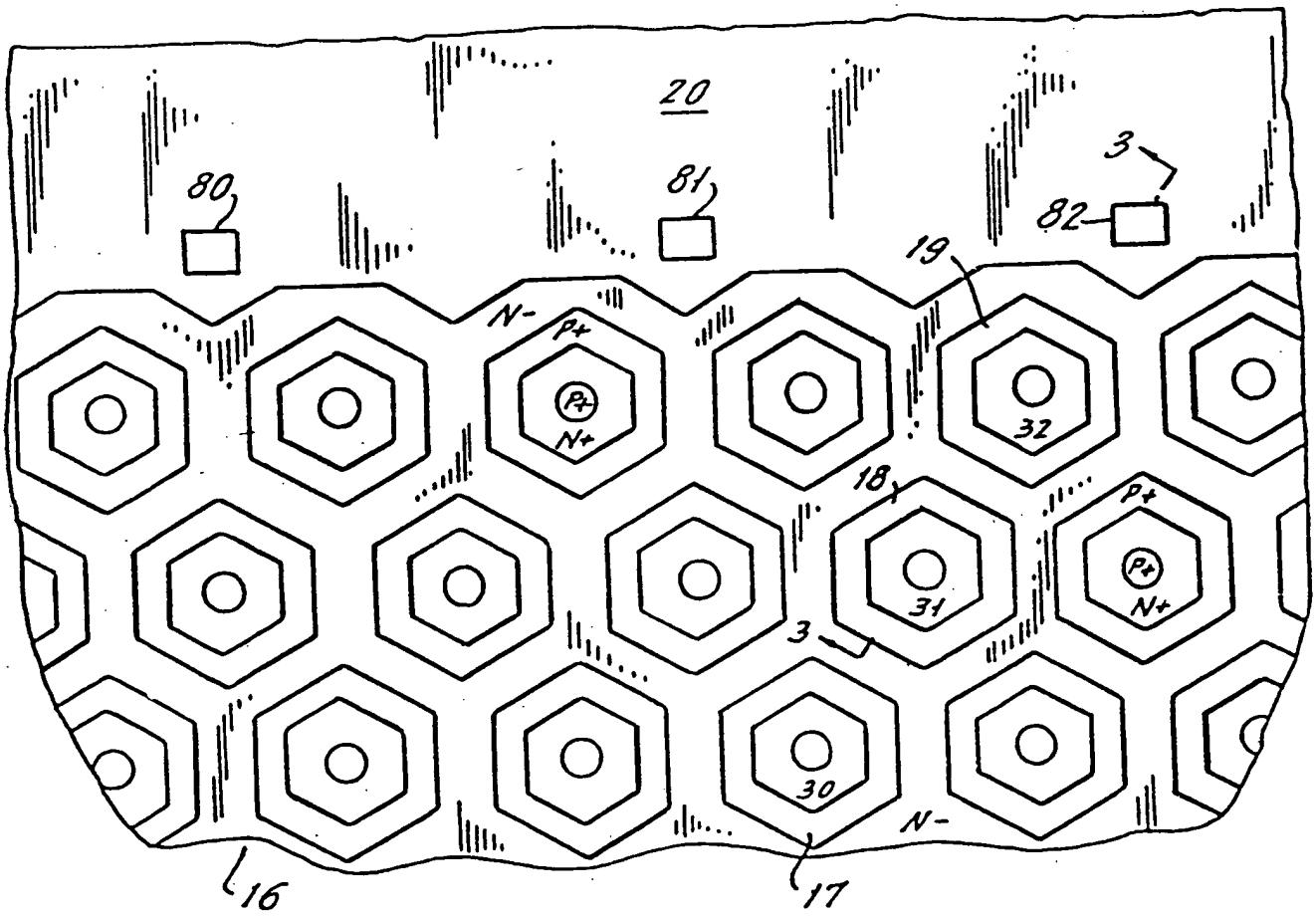
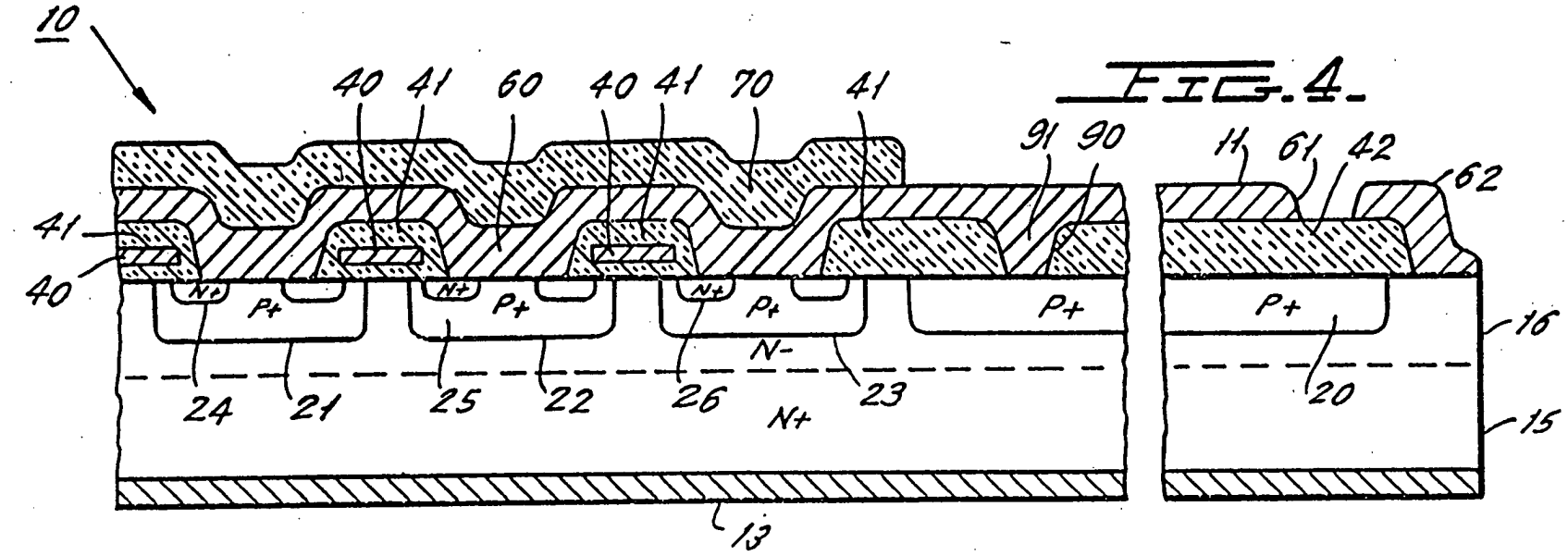
4
SOURCE PAD
11
A
10
GATE PAD
12

FIG. 2


20
80
81
3
82
19
N-
P+
P+
N+
32
18
P+
P+
N+
31
3
30
N-
16
17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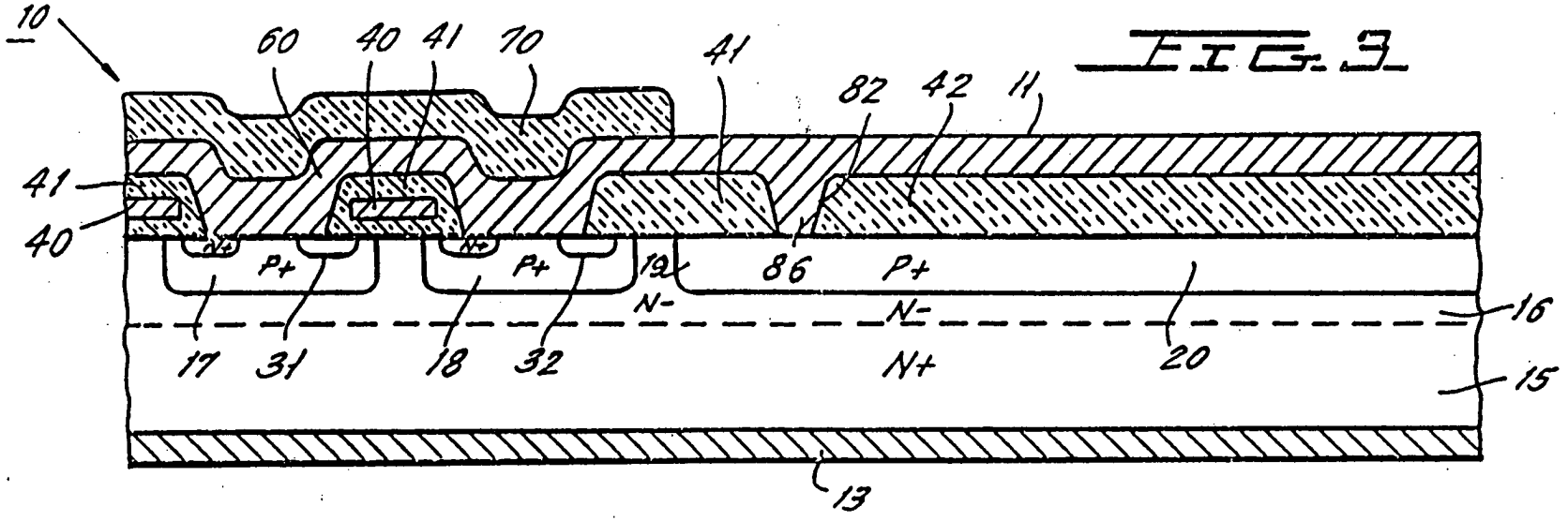
40
41
70
41
91
90
11
61
42
62
41
40
N+
P+
N+
P+
N+
P+
P+
P+
16
N-
24
21
25
22
26
N+
23
20
15
13

FIG. 4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60
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70
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82
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11
41
40
N+
P+
N+
P+
19
86
P+
16
N-
N-
17
31
18
32
N+
20
15
13

FIG. 3

2/2

SPECIFICATION

High power MOSFET with direct connection from connection pads to underlying silicon

This invention relates to high power metal oxide semiconductor field effect transistors, and more specifically relates to a novel connection of the peripheries of the electrode pads of such devices directly to the underlying silicon to prevent failure of the device when it is operated in a diode mode.

High power metal oxide semiconductor field effect transistors (MOSFETS) which typically may be vertical conduction devices are well known. Commonly, such devices consist of a very large number of cells, which might be greater than 5,000, on a single small chip area with the devices all connected in electrical parallel. Typically, each cell may consist of a base region diffused into one surface of the main wafer or chip. A source region is formed within each base region and defines a conventional MOSFET channel. Each MOSFET channel underlies a conventional MOSFET gate which may be formed of polysilicon. The gate elements are connected together and can be connected to a common gate electrode pad, which is accessible on one surface of the chip, to which convenient gate connection can be made. Similarly, each of the sources is conventionally connected to a single sheet electrode which overlies the entire chip surface and which extends to a source electrode pad for making easy connection to the source of the device. The electrode pads are normally supported atop an oxide layer which is disposed between the pad surface and the underlying silicon wafer or chip surface. Conventionally, the silicon beneath the pad regions is of the same conductivity type of the cell base regions.

The source electrode which contacts each of the sources within each of the base regions also makes contact to a central portion of the cell base region. Consequently, the overall device acts as a single junction device or diode when the source electrode is one polarity, but as a MOSFET when the source electrode is of the other polarity. It has been found that MOSFET devices of the above structure experience failure during operation in a diode mode under particular circuit conditions. Upon inspection, it was discovered that failure occurred in the cell elements around the periphery of the electrode pads.

In analyzing the above problem, it is recognized that when the device operates as a MOSFET, it operates as a majority carrier device so that each of the cells which are connected in parallel with one another will carry only its appropriate share of the load current. However, when the device is operated as a diode, it is operated as a minority carrier device and there is a tendency for diodes which carry more current than others to become locally heated. Thus, they tend to conduct still more current and this process continues until certain individual cells carry sufficient current to destroy the device. It has been discovered that this tendency for "hogging" current is more pronounced for those cellular elements which are disposed adjacent the edges of the connection pads of the device. The reason for this has been recognized to be that the region beneath the pads tends to weakly inject carriers into the underlying region, during the operation of the device. When the device is then operated as a diode, the carriers injected into the region under the pad periphery are very quickly collected by adjacent cell elements operating as individual parallel diodes since these cell elements are firmly connected to the source electrode. The regions under the pads, however, cannot collect this current since they are not firmly connected to the source electrode. Consequently, those diodes immediately adjacent the pad edges become immediately more highly conductive than cells remote from the pad periphery and they carry an even greater share of the current of the overall device until the cells fail.

Accordingly, a first aspect of the present invention provides a metal oxide semiconductor field effect transistor comprising a semiconductor wafer, a plurality of base regions of one conductivity type symmetrically and laterally distributed over at least a portion of the area of one surface of said wafer; a respective source region of the other conductivity type in each of said base regions and laterally spaced from the periphery of their said respective base regions to define respective channel regions capable of inversion within its said respective base region; an insulation layer overlying each of said channel regions and extending over a connection pad region; and over each of said channel regions; a source electrode means in contact with each of said source regions and with each of said base regions; a drain electrode connected to the opposite surface of said wafer; an enlarged area source electrode pad connected to said source electrode means and overlying said insulation layer in said connection pad region; an enlarged area base region of said one conductivity type underlying said source electrode pad; and connection means electrically connecting at least portions of the periphery of said source electrode pad to said enlarged base region beneath said pad whereby said enlarged base region can efficiently collect minority carriers when said transistor operates as a diode.

A second aspect of the present invention provides a semiconductor device consisting of a plurality of separate parallel-connected diode type elements formed in a common substrate of one conductivity type and an enlarged area electrode pad connected to each of said diode type elements; each of said diode type elements including a diffusion region of the other conductivity type which forms a junction within said substrate; a further diffusion region of said other conductivity type underlying said electrode pad; a thin insulation layer separating said insulation layer and said substrate in the area of said electrode pad; and a plurality of electrical connection regions extending from said electrode

pad, and formed around at least portions of the periphery of said source electrode which surrounds said gate electrode pad means to said second enlarged base region.

With the discovery of the problem as stated above, wherein device failure is precipitated during the diode mode of operation by failure of the cell elements surrounding the pad, a plurality of direct connection points were made from the source electrode to the underlying silicon surface completely around the periphery of each of the source and gate pads. By making the direct connection, the base type material immediately under the pads becomes a very efficient collector of minority carriers which were previously injected beneath the pads during operation of the overall device as a diode. Consequently, these carriers are immediately swept up by the region beneath the pads rather than by adjacent cell elements so that the adjacent cell elements do not become more efficient diodes than the others, which would lead to their ultimate failure during operation in the diode mode.

The invention will be further described by way of example with reference to the accompanying drawings which:

Figure 1 is a plan view, greatly enlarged, of a typical MOSFET having a source pad and gate pad accessible for connection to source and gate leads on the upper surface of the device;

Figure 2 is an enlarged view of the junction pattern of the silicon surface of the silicon chip of Figure 1 and is a view greatly enlarged of the area within the circle marked "A" in Figure 1;

Figure 3 is a cross-sectional view of Figure 2, taken across the section line 3—3 in Figure 2 and further shows the electrodes atop the silicon surface of Figure 2;

Figure 4 is a view similar to that of Figure 3, but shows the pad at the top and edge of the chip.

Referring first to Figure 1, there is shown a semiconductor chip 10. In general, the chip shown in Figure 1 can have a length of about 100 mils and a width of about 100 mils and will contain therein greater than 6,000 individual MOSFET cells which are connected in parallel, as will be later described.

The chip surface contains a source pad 11 which is an exposed enlarged metallic surface which can be connected to a source wire lead. There is also a gate pad 12 which similarly is an enlarged exposed metallic surface to which a gate lead can be attached. The bottom surface of the device receives a drain electrode 13 (Figures 3 and 4).

The configuration of the individual MOSFET cells on the upper surface of the wafer or chip of Figure 1 is shown in Figures 2, 3 and 4 for the case of a hexagonal cell geometry. Note that any closed cell geometry could be used for the individual cells such as rectangular or square configurations. The device disclosed in Figures 2, 3 and 4 is an N-channel device but it will be apparent to those skilled in the art that a P-channel device could also employ the invention to be described.

In the example given herein, the chip consists of an N+ body of silicon 15 which has an N— epitaxial layer 16 grown thereon. The N— layer 16 contains a plurality of base diffusions such as the P+ base diffusions 17, 18 and 19 which are shown as having a hexagonal geometry. Any other geometry could be used. Layer 16 also has the P+ diffusion 20 which is formed simultaneously with the bases. The P+ diffusion 20 underlies the complete area of the source pad 11 in Figure 1. A similar P+ diffusion (not shown) underlies the full extent of the gate pad 12 in Figure 1.

Each of the P+ cells such as cells 17, 18 and 19 receives a hexagonal source diffusion shown as source diffusions 30, 31 and 32, respectively. A similar arrangement of cells is shown in Figure 4 where hexagonal P+ cells 21, 22 and 23 receive source diffusions 24, 25 and 26, respectively. The annular regions between the exterior of the source diffusions 24, 25, 26, 30, 31 and 32 and the base regions 21, 22, 23, 17, 18 and 19, respectively, define respective hexagonal channels. Each of these channels is covered by a respective gate electrode, shown in Figures 3 and 4 as the polysilicon gate lattice 40 which has lattice sections overlying each of the channels. The polysilicon gate lattice 40 is supported above the surface of the silicon chip 10 and is, in effect, encapsulated in a lattice configured silicon oxide layer 41. Note that the layer 41 has an extending region 42 which extends over the surface of the silicon and underlies the full area of the source electrode pad 11. Similarly, the oxide 42 will also underlie the conductive material of the gate pad 12.

The insulation layer 41 may consist of several insulation layers. It can, for example, include a very thin silicon dioxide layer, for example, 1,000 Angstroms directly beneath the gate segments 40. The upper layer of encapsulating insulation layer 41 can be a reflowed silox formed above and around the sides of gate lattice 40 to ensure good insulation of the gate 40 from the source electrode. Note that the insulation layer 41 extends over only a portion of the outer periphery of the source diffusions 30, 31 and 32 in Figure 3 and 21, 22 and 23 in Figure 3 to enable subsequent contact to these source regions.

An aluminum sheet electrode 60, shown in Figures 3 and 4, then overlies the full surface of the chip and makes contact to the inner periphery of each of the source diffusions and to the central exposed P+ region of their respective bases. Sheet 60 is divided into a smaller gate pad section 12 and the larger source electrode which extends to the source pad 11. Gate lattice 40 is appropriately connected to gate pad region 12.

Note that the source electrode extends over the full extent of oxide layer 42. Note also that at the edge of the chip, shown in Figure 4, the pad portion 11 of electrode 60 falls short of the edge of the chip at edge section 61. A channel stopper

electrode 62 then is provided in the usual manner and is connected to the underlying N— material and to the drain electrode 13.

The entire upper surface of the device, except for the source and gate pads, is covered by an oxide layer or other suitable insulation layer 70 to protect the upper surface of the device. This upper layer 70 is removed in the area of the source pad 11, as shown in Figures 1, 3 and 4 and is also removed in the area of the gate pad 12.

In prior art devices of this type and particularly in prior art vertical conduction high power MOSFET devices employing a plurality of parallel-connected cells, it has been found that cells sometimes fail in the area adjacent the boundary of the source pad 11 or gate pad 12 when the device is operated in a diode mode. Thus, the device shown in Figures 3 and 4 can operate in a MOSFET mode or in a diode mode, depending upon the potential of the source 60 and of the drain 13. When the drain 13 is positive and the source 60 is negative, device conduction is controlled by the MOSFET mode. Thus, when a suitable potential is applied to the gate 40, the channel region between the external periphery of the individual sources and the outer periphery of their respective bases will become inverted so that a conduction path is formed from drain 13 to source 60 when a gate potential is applied. However, when the source and drain potentials are reversed and the source electrode 60 is positive, the entire device operates as a forward-biased diode having the diode junction formed between the P+ base regions and the N— body regions.

When the device is operating as a diode, each of the 6,000 or more cells of the device conduct current in parallel. The failure of diode elements surrounding the periphery of the connection pads was unexplained until it was recognized that the P+ region 20, which was very weakly connected to the pad 11, was weakly injecting minority carriers into the N— body during the time that the device acted as a MOSFET transistor. When the potential between the source electrode 60 and drain electrode 13 reversed, the junction formed by region 20 was unable to efficiently collect these injected carriers, so that these carriers preferentially were swept into the individual cells surrounding the pad such as the cells including sources 32 and 26 in Figures 3 and 4, respectively. These cells could readily collect the carriers which were previously injected from the region 20 since they are very firmly connected to the source electrode 60. Consequently, they became more efficient diodes than the other diodes farther removed from the pad 11. Since the device operates as a minority carrier device when operating as a diode, these cells tended to rapidly conduct increasingly more than their share of the current flowing through the device until they failed.

In accordance with the invention, a direct electrical connection is made from the source electrode 60 at the periphery of pad 11 to the periphery of the underlying P+ region 20 to make it a more efficient minority carrier collector when the device is operated in the diode mode. Similarly, a connection is made from the source electrode 60 at the periphery of gate pad 12 to the underlying P+ region.

For example, as shown in Figures 2, 3 and 4, a plurality of openings are formed in the oxide 42 at regions identified particularly in Figure 2 by the numerals 80, 81 and 82 and which are disposed around the periphery of the pad. Thus, during the time the metal electrode 60 is applied over the surface of the device, connection will be made, as shown by the connection point 86 in Figure 3, at region 82 to the P+ region 20. A similar opening 90 is formed at the region of the source pad 11 through which the section of Figure 4 has been taken and a connection 91 is made from the source electrode 60 to the underlying P+ region 20 by the connection point 91.

The number or spacing of connection points is not critical. It has been found satisfactory to have a connection point at a point adjacent approximately every other cell element. A similar arrangement of connection points from the source electrode surrounding the outer periphery of the gate pad 12 to the underlying P+ region beneath the gate pad and through the spacing oxide is also provided but is not shown.

In an exemplary device, the source pad 11 had the dimensions of 30 mils by 25 mils. About 40 connection points surrounded the periphery of the source pad which had a separation of about 3 mils from one another. The connection points can be inwardly spaced from the effective edge of the pad by a distance approximately equal to the width of a cell which might be approximately 1 mil.

Although the present invention has been described in connection with a preferred embodiment thereof, many variations and modifications will now become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

CLAIMS

1. A metal oxide semiconductor field effect transistor comprising a semiconductor wafer, a plurality of base regions of one conductivity type symmetrically and laterally distributed over at least a portion of the area of one surface of said wafer; a respective source region of the other conductivity type in each of said base regions and laterally spaced from the periphery of their said respective base regions to define respective channel regions capable of inversion within its said respective base region; an insulation layer overlying each of said channel regions and extending over a connection pad region; and conductive gate means disposed atop said insulation layer over each of said channel regions a source electrode means in contact with each of said source regions and with each of said base regions; a drain electrode connected to the opposite

surface of said wafer; an enlarged area source electrode pad connected to said source electrode means and overlying said insulation layer in said connection pad region; an enlarged area base region of said one conductivity type underlying said source electrode pad; and connection means electrically connecting at least portions of the periphery of said source electrode pad to said enlarged base region beneath said pad whereby said enlarged base region can efficiently collect minority carriers when said transistor operates as a diode.

2. A transistor as claimed in claim 1, wherein said connection means comprises a plurality of generally equally spaced conductive projections from said source pad which extend through said insulation layer and are connected to said enlarged base region.

3. A transistor as claimed in claim 1 or 2, wherein said base regions and said source regions have respective identical structures.

4. A transistor as claimed in claim 1, 2 or 3, wherein said insulation layer consists of silicon dioxide.

5. A transistor as claimed in any one of claims 1 to 4, wherein said source electrode means and said source pad consist of a single sheet of conductive material.

6. A transistor as claimed in any of claims 1 to 5, wherein said one conductivity type is the P type.

7. A transistor as claimed in any of claims 1 to 6, wherein the outer periphery of said base regions and of said respective source regions is polygonal.

8. A transistor as claimed in claim 7 wherein said outer periphery is hexagonal.

9. A transistor as claimed in any of claims 1 to 8, which further includes an enlarged area gate electrode pad means on said one surface which is connected to said conductive gate means; said insulation layer underlying said gate electrode pad means; and a second enlarged base region underlying said insulation layer beneath said gate electrode pad means; and second connection means electrically connecting at least portions of the periphery of said source electrode which surrounds said gate electrode pad means to said second enlarged base region.

10. A semiconductor device consisting of a plurality of separate parallel-connected diode type elements formed in a common substrate of one conductivity type and an enlarged area electrode pad connected to each of said diode type elements; each of said diode type elements including a diffusion region of the other conductivity type which forms a junction within said substrate; a further diffusion region of said other conductivity type underlying said electrode pad; a thin insulation layer separating said insulation layer and said substrate in the area of said electrode pad; and a plurality of electrical connection regions extending from said electrode pad, and formed around at least portions of the periphery of said source electrode which surrounds said gate electrode pad means to said second enlarged base region.

11. A semiconductor device as claimed in claim 10 wherein each of said diode type elements is a portion of a respective metal oxide semiconductor field effect transistor type device.

12. A semiconductor device as claimed in claim 11 wherein there is a single sheet source electrode connected to each of said metal oxide semiconductor field effect transistor type devices; said electrode pad comprising an extension of said source electrode.

13. A metal oxide semiconductor field effect transistor substantially as herein described with reference to, and as shown in, the accompanying drawings.

14. A semiconductor device substantially as herein described with reference to and as shown in the accompanying drawings.

Printed in the United Kingdom for Her Majesty's Stationery Office, Demand No. 8818935, 10/1984. Contractor's Code No. 6378.
Published by the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.